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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,345	09/18/2003	Jicheng Yang	2269-6383.2US (99-0294.02	8177

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JOSEPH A. WALKOWSKI
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, UT 84110

EXAMINER	
PERKINS, PAMELA E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,345	YANG, JICHENG	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-19 and 30-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-19 and 30-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/420,817.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application papers on 18 September 2003. Claims 12-19 and 30-37 are pending; claims 1-11 and 20-29 have been cancelled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 30 and 33-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. (5,239,198).

Lin et al. disclose a method of forming a multi-chip module where a first chip (27) is coupled to a first side of a support structure (12); coupling a second chip (20) to a second side of the support structure (12) (col. 3, lines 31-67); causing the support structure (12) to extend outwardly beyond the first chip (27) (col. 4, lines 35-63); providing solder ball pads (14/16) and solder balls (32) on the portion of the structure (12) extending outwardly beyond the first and second chips (27, 20), extend outwardly beyond four edges of the first chip (27) (Fig. 5; col. 6, lines 29-47); and the pads (14/16) electrically coupled to the first and second chips (27, 20) (Fig. 4; col. 4, line 64 thru col. 5, line 11). Lin et al. further disclose the second chip (20) including bump bonding (25/26) to the second side of the support structure (12) (Fig. 2) (col. 4, lines 12-29). Lin

et al. also disclose coupling the first and second chips (27, 20) to the solder ball pads (14/16) on the portion via traces (18) extending through the structure (12) (col. 3, lines 31-53).

Claims 30 and 33-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Egawa (6,222,215).

Egawa discloses a method of forming a multi-chip module where a first chip (17) is coupled to a first side of a support structure (10/30); coupling a second chip (11) to a second side of the support structure (10/30); causing the support structure (10/30) to extend outwardly beyond the first chip (17) (col. 4, lines 1-31); providing solder ball pads (not shown) on the portion of the structure (10/30) extending outwardly beyond the first and second chips (17, 11), extend outwardly beyond four edges of the first chip (17); and the pads (not shown) electrically coupled to the first and second chips (17, 11) (col. 5, lines 8-41). Egawa further discloses the second chip (11) including bump bonding (21/32) to the second side of the support structure (10/30) (col. 4, lines 32-53). Egawa also discloses coupling the first and second chips (17, 11) to the solder ball pads (not shown) (col. 4, lines 1-53).

Egawa discloses aligning the first and second chips (17, 11) over one another so as to form an extension of the support structure (10/30) that extends outwardly beyond the chips (17, 11) and completely around the module (Fig. 1a; col. 3, lines 47-64). Egawa further discloses filling a region between the chips (17, 11) with an encapsulant (33) (Fig. 4; col. 5, lines 42-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12-18, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egawa in view of Bertin et al. (6,300,687).

Egawa does the subject matter claimed above except adhesively securing a first chip to a first surface of a laminate layer and wire bonding the first chip to a second surface of the laminate layer.

Bertin et al. disclose a method of forming a multi-chip module where a first chip (60) is adhesively secured (58) to a first surface of a laminate layer (45); inverting the assembly of the laminate layer (45) and the first chip (60); wire bonding (53) the first chip (60) to a second surface of the laminate layer (45); and positioning the first chip (60) on the laminate layer (45) so that at least a portion of the laminate layer (45) extends outwardly beyond the first chip (60) (col. 4, lines 31-39). Bertin et al. further disclose forming a passage through the laminate layer (45) and forming wire bonds (53) from the first chip (60) through the passage to the second surface of the laminate layer (45) (Fig. 8).

Since Egawa and Bertin et al. are both from the same field of endeavor, a method of forming a multi-chip module, the purpose disclosed by Bertin et al. would have been recognized in the pertinent art of Egawa. Therefore, it would have been

obvious to one ordinary skill in the art at the time the invention was made to modify Egawa by adhesively securing a first chip to a first surface of a laminate layer and wire bonding the first chip to a second surface of the laminate layer as taught by Bertin et al. to decrease inductance (col. 1, lines 44-64).

Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egawa in view of Bertin et al. as applied to claim 12 above, and further in view of Lin et al.

Egawa in view of Bertin et al. disclose the subject matter claimed above except forming a passage through said laminate layer and forming wire bonds from the first chip through the passage to the second surface of the laminate layer.

Lin et al. disclose a method of forming a multi-chip module where a first chip (27) is coupled to a first side of a support structure (12); coupling a second chip (20) to a second side of the support structure (12) (col. 3, lines 31-67); causing the support structure (12) to extend outwardly beyond the first chip (27) (col. 4, lines 35-63); providing solder ball pads (14/16) and solder balls (32) on the portion of the structure (12) extending outwardly beyond the first and second chips (27, 20), extend outwardly beyond four edges of the first chip (27) (Fig. 5; col. 6, lines 29-47); and the pads (14/16) electrically coupled to the first and second chips (27, 20) (Fig. 4; col. 4, line 64 thru col. 5, line 11). Lin et al. further disclose the second chip (20) including bump bonding (25/26) to the second side of the support structure (12) (Fig. 2) (col. 4, lines 12-29). Lin et al. also disclose coupling the first and second chips (27, 20) to the solder ball pads

(14/16) on the portion via traces (18) extending through the structure (12) (col. 3, lines 31-53).

Since Egawa and Lin et al. are both from the same field of endeavor, a method of forming a multi-chip module, the purpose disclosed by Lin et al. would have been recognized in the pertinent art of Egawa. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Egawa by forming a passage through the support structure as taught by Lin et al. to save board space (col. 2, lines 10-50).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800